PATHKEY AGM 2026 / ASX: PKY

PathKey

What has happened. What is proven. What comes next.

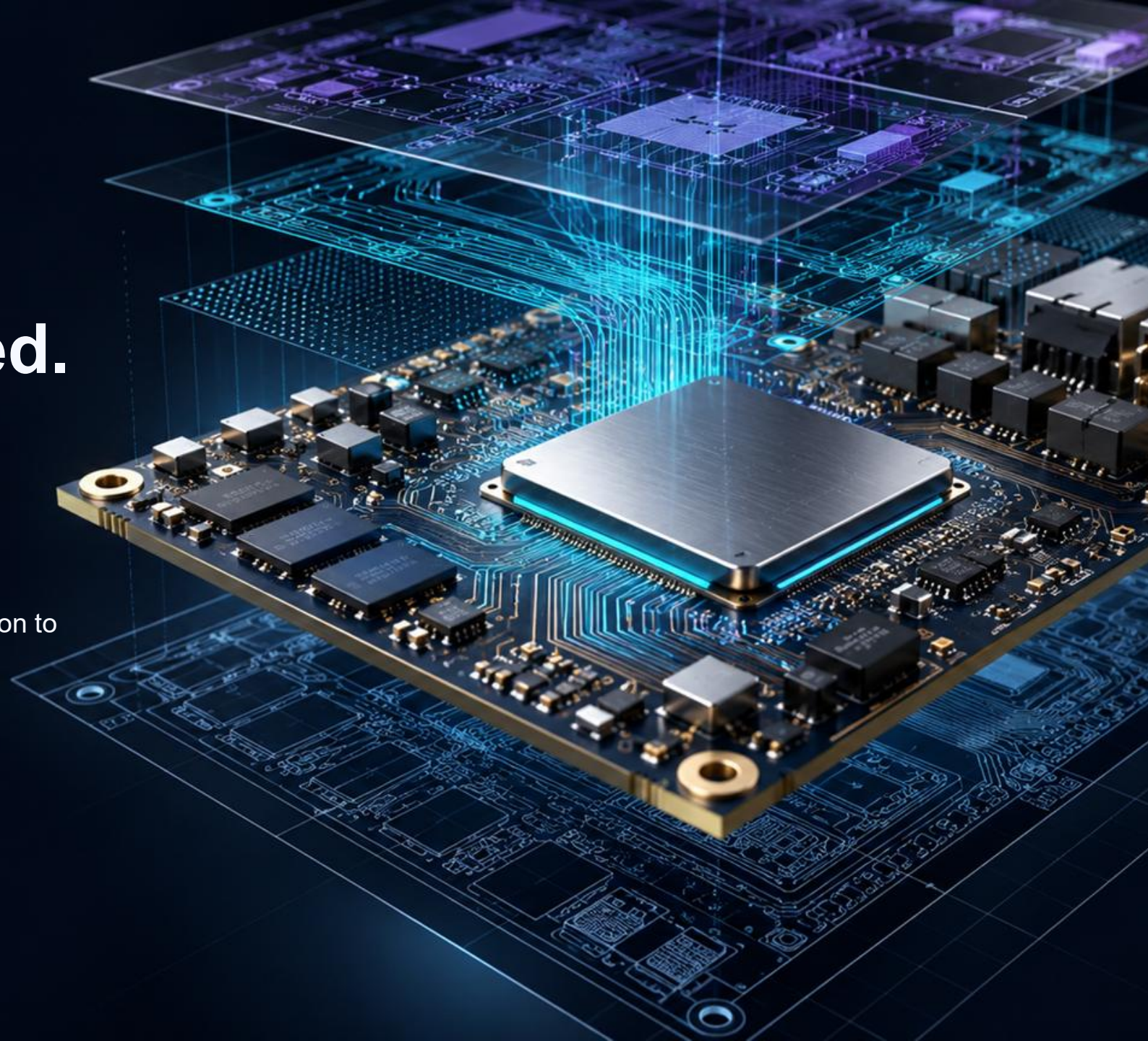
Chipforge. Engineering intelligence that brings silicon to market at the speed of software.

AGM investor webinar / 5 November 2026

Andrew Farnsworth, Group CEO

Chipforge

TrialKey



Disclaimer

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Statements about future product releases, tool chain support, the secure infrastructure platform, the fine tuned model, custom silicon, customer engagements, revenue and funding are forward-looking. They reflect current intentions and assumptions, give no confirmed dates, and depend on technical progress, customers, competition, staffing and funding. Actual results and timing may differ materially. They are not guarantees or forecasts, and no assurance is given that they will be achieved.

EVIDENCE AND FINANCIAL INFORMATION

Internal test and benchmark results reflect specific test conditions, are unpublished unless stated, and are not universal performance claims. Comparison figures come from published sources on the dates shown. TrialKey model outputs are exploratory predictions, have not been assessed by subject matter experts and are not results. The design-iteration comparison is illustrative only. Financial information is historical, in Australian dollars and unaudited unless stated. Quarters of funding are as reported in Appendix 4C. Vendor and tool names identify the tool ecosystem and imply no partnership, certification or compatibility. Trademarks belong to their owners.

AUTHORISATION

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Since the last AGM, several key moments

29 Apr 2026
Announced Chipforge Acquisition

23 Jun 2026
Acquisition completed following shareholder approval

11 Aug 2026
Chipforge contract for proof of value design

12 Aug 2026
Raised A$2.8m and appointed Sam Weiss as strategic advisor

10 Sep 2026
Prof. Anupam Chattopadhyay appointed to Advisory Board

Oct 2026
Proven end to end. Independent validation of Chipforge Platform by subject matter expert. Platform used without any prior knowledge to create hardware designs from intent to FPGA implementation. Independent user confirmation that Platform passed verification tests without any team input or assistance

Nov 2026
Production systems built, ready for post-MVP release

Pathkey builds AI that is core to two very large industries

PathKey — ASX Listed, code ASX: PKY

ACQUIRED · JUNE 2026

Chipforge

SEMICONDUCTORS CHIP DESIGN

US$22.0bn of EAD software sold in 2025, growing 10% a year. A design layer for all EDA chip design tools.

Engineers explains and inputs their intent. Chipforge designs, tests and verifies it, from FPGA through to ASIC.

EXISTING

TrialKey

CLINICAL TRIALS

The top 20 drug companies spent US$145bn on R&D in a year. 76% of trial plans change after the trial starts.

AI that assesses a clinical-trial design before the money is committed.

Experts stay in charge of the decision.

Sources: SIA / WSTS, 6 Feb 2026; Deloitte, top-20 biopharma R&D spend 2022-23; Tufts CSDD, 2024.

Chipforge

Custom chip design is a chain of specialist handoffs. Chipforge runs the whole flow

THE PROBLEM

Specify, architect, design, verify, implement, test on hardware. Each step has its own engineering specialist and its own tool.

Every change goes back through the chain. Three in four chip projects run late. Teams carry two or more verification engineers for every designer. Companies that need custom hardware either carry that whole team or do not build.



CHIPFORGE

The design layer across the whole flow.

The engineer brings the design requirement for the chip. Chipforge takes it through design, test, fix and implementation to a verified design on the target hardware, with every step recorded. Iterations happen inside Chipforge, not through a chain of handoffs.

Targeted redesign and re-verification when requirements change.

The engineer directs the outcome.

Intent to hardware
From Design idea to a verified design on target hardware.

Your tools, your choice.
Verified by the tools the industry already trusts. AMD, Altera, Lattice and, later, the custom-silicon tools.

Inside your walls
Built to run on the customer's own computers when designs cannot leave the building.

Sources: Wilson Research Group functional verification studies, 2022 and 2024 (Siemens EDA). 75% of IC/ASIC projects behind schedule in 2024; verification to design engineer ratio up to 5 to 1 in processor projects.

Chipforge

Chipforge technology works, it is proven against industry benchmarks

Validated

It works end to end, without us in the room
An independent user took multiple designs from intent through to deployment on a target FPGA and confirmed it tested, without our help.

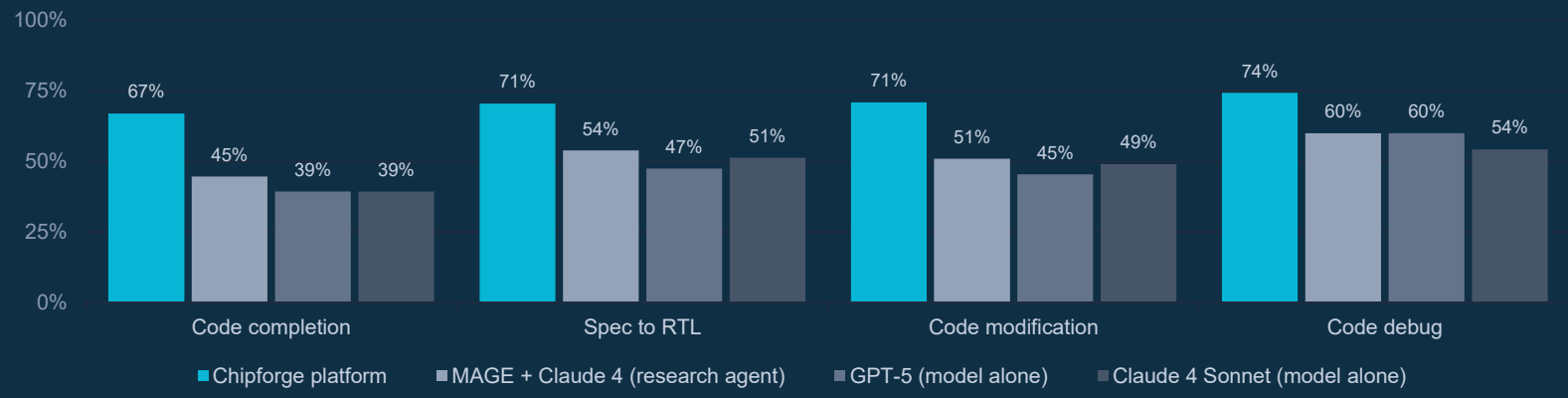
Benchmarked

Proven against core industry design problems & benchmarks
The platform has been tested across NVIDIA's public CVDP chip-design benchmarks, four task types, against published results.

Pre-Release

Staging for Production
The production environment is live, with continuous integration, monitoring and alerting, readying for the post-MVP release.

NVIDIA CVDP BENCHMARK · 1ST PASS RATE BY TASK, %



+14 to +28% improvement

WHAT EACH TASK MEANS

- **CODE COMPLETION —** Fill missing RTL in a partial module.
- **SPEC TO RTL —** Build working RTL from a natural-language specification.
- **CODE MODIFICATION —** Update supplied RTL to meet revised requirements.
- **CODE DEBUG —** Find and fix defects in buggy RTL until tests pass.

Sources: NVIDIA CVDP benchmark (arXiv 2506.14074). GPT-5, Claude 4 Sonnet and MAGE results from NVIDIA ACE-RTL, arXiv 2602.10218

Chipforge

Chipforge enables engineers to design and iterate multiple projects in the time current tools take to create one.

ILLUSTRATIVE The same team and the same window of time, two ways of working. Durations are for illustration, not a customer result.

EXISITING EDA TOOL CHAIN FLOW · ONE DESIGN

Specify	Design	Verify	Implement	Test on hardware	1 design	DONE

CHIPFORGE · THE SAME WINDOW AND WHY WE CAN DO IT FASTER

Design 1 verified on hardware	Design 2 or variation verified on hardware	Design 3 or variation verified on hardware	Design 4 or variation verified on hardware	4 designs	DONE

Why? - Tests are written and run inside the platform	Why? - Failures are fixed in the loops, no handoff between teams	Why? - Every step is recorded, so a change re-verifies only what changed	Why? - A variation is a change, not a new project

Same engineers, same capability, same window of time. Chipforge removes the handoffs and full re-verification that make one design take so long, so the team can run several designs at once and take the best one forward to custom silicon, each verified on the way.

Chipforge

One design, multiple tool chains. The design belongs to the customer

THE CUSTOMER'S DESIGN AND ITS RECORD
Intent, code, tests, evidence and reasons. Owned by the customer.

CHIPFORGE · THE DESIGN LAYER
Designs, tests and verifies the customer's intent. Change the target hardware and the same design and intent are rerun through the platform, re-targeted and re-verified for the new tool chain. A platform run, not a new project.

FPGA · HARDWARE FLEXIBILITY · TRANSLATOR STATUS

AMD	Altera	Lattice	Microchip
Vivado **Built**	Quartus **Built**	Radiant **Next**	Libero **Next**

The same verified intent and code carried forward. Proven on FPGA, iterated, then regenerated and re-verified for custom silicon when the volume justifies it.
No lock-in to one vendor's parts, prices or roadmap.

In 2026 Synopsys, Cadence, Siemens and AMD each launched AI agents inside their own tools, and startups in the space raised over US$500m. The market is validated. Chipforge sits above the tool chains and works across them.

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CUSTOM SILICON · THE SAME PLATFORM · ROADMAP

Synopsys	Cadence	Siemens
Fusion Compiler, VCS **Roadmap**	Genus, Innovus, Xcelium **Roadmap**	Questa, Calibre **Roadmap**

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Chipforge

Faster designs, more productive engineers

BUILT

The design intent graph

A live, typed record of every module, port, signal, parameter and clock domain—built from specs, diagrams and conversation. Every stage reads and writes to the same graph, exposing contradictions before code and mismatches before silicon.

IN TRAINING

The fine-tuned model

Our dedicated chip-design model fine-tuned and trained across the full EDA workflow. It runs inside the customer environment, so proprietary designs never need to reach an external AI service. Preserving security, control and data ownership.

GROWING

The knowledge layer

Every verified run adds designs, methods and rationale to the customer's record. Knowledge stays with the organisation when engineers move on, and new team members can pick up context directly from the tool.

EXTENDING

The tool translators

Integration layers connect Chipforge to FPGA tools from AMD, Altera and Microchip, then extend to custom-silicon workflows from Synopsys, Cadence and Siemens. They translate intent into each vendor's formats, commands and checks.

PROTECTED BY

Ongoing research and development is identifying unique IP that Chipforge will aim to protect.

Chipforge

APAC region wants full control over chip design. Chipforge will enable sovereign control, wherever the data is hosted

ASIA PACIFIC · FROM MAKING CHIPS TO DESIGNING THEM

~ 1 in 10
of the world's chips are made in Singapore

S$800m
Singapore program naming IC design as a focus, 2026

50,000
chip design engineers Vietnam targets by 2030

¥2.35tn
Japan's commitment to Rapidus, 2nm by 2027

AUSTRALIA - SOVEREIGN CAPABILITY

A national security priority

The 2026 Integrated Investment Program and the National Semiconductor Roadmap now being written treat sovereign chip capability as national security.

All of it runs on overseas tool chains.

DEPLOYED WHERE THE DATA HAS TO LIVE - THE CUSTOMER CHOOSES

Public cloud
Open infrastructure, now in MVP

In Pre-release · Target Chipforge Studio v1 Q3 FY27

Private cloud
Whole platform and fine-tuned model in the customer's cloud or data centre

In development · FY 2028

Appliance
Self-contained and air-gapped, for sovereign and secure programs

In development · FY 2028

You cannot hire your way to a chip, and neither can this region. The world is more than a million chip engineers short by 2030, and the gap is widest where the chips are made.

Sources: SG Semiconductor launch, A*STAR and EDB, 2026; SEMI Southeast Asia, June 2026; Vietnam semiconductor strategy, September 2024; Japan Rapidus funding, 2026; Australia 2026 Integrated Investment Program; S3B National Semiconductor Roadmap announcement, March 2026; Deloitte, global semiconductor talent shortage.

Chipforge

How Chipforge gets paid, and who pays

WHO PAYS

Product and hardware developers

Companies building products that need custom hardware, from machines and robots to drones and devices. Most have no chip team.

Edge and sensing systems

Data has to be processed where it is produced, and general-purpose silicon consumes too much power and is too expensive.

Design houses and services firms

They design for the first two. More projects than engineers; margin is designs shipped per engineer.

Sovereign capability

Defence, government and high-security programs. Designs cannot leave the building and cleared engineers are the scarcest of all.

US$22bn a year is the chip design tools market, growing about 9 to 10% a year. Asia Pacific is about 40% of it and growing 20% a year, the fastest of any region. That is the market Chipforge sells into.

HOW THEY PAY · THE LADDER

01
Proof of value

Fixed price for a scoped design on the customer's own requirement.

02
Paid programs

Stage One: The same customer brings more designs. Further project fees or usage charges.

Stage Two: Cloud on consumption with flexible licensing, or in-house on a multi-year licence. The customer chooses and can move between them.

03
Custom silicon and Embedded platform

The same verified design taken through to custom silicon. Project fees for the design work, embedding into the operating design workflow for the customer and a licence on the IP Chipforge supplies.

Sources: ESD Alliance (SEMI) EDA market statistics, Q3 2025, US$5.6bn for the quarter, Asia Pacific US$2.22bn up 20.5%;

Clinical trials become costly because the plan changes after the money is committed

9 in 10
change their study plans

2 in 3
finish later than first estimated

Nearly half
recruit fewer people than planned

TrialKey analysis of 27,178 trials. Independent research puts plan changes at three in four; our own dataset puts it at nine in ten.

These problems increase cost and the risk of a trial stopping early.

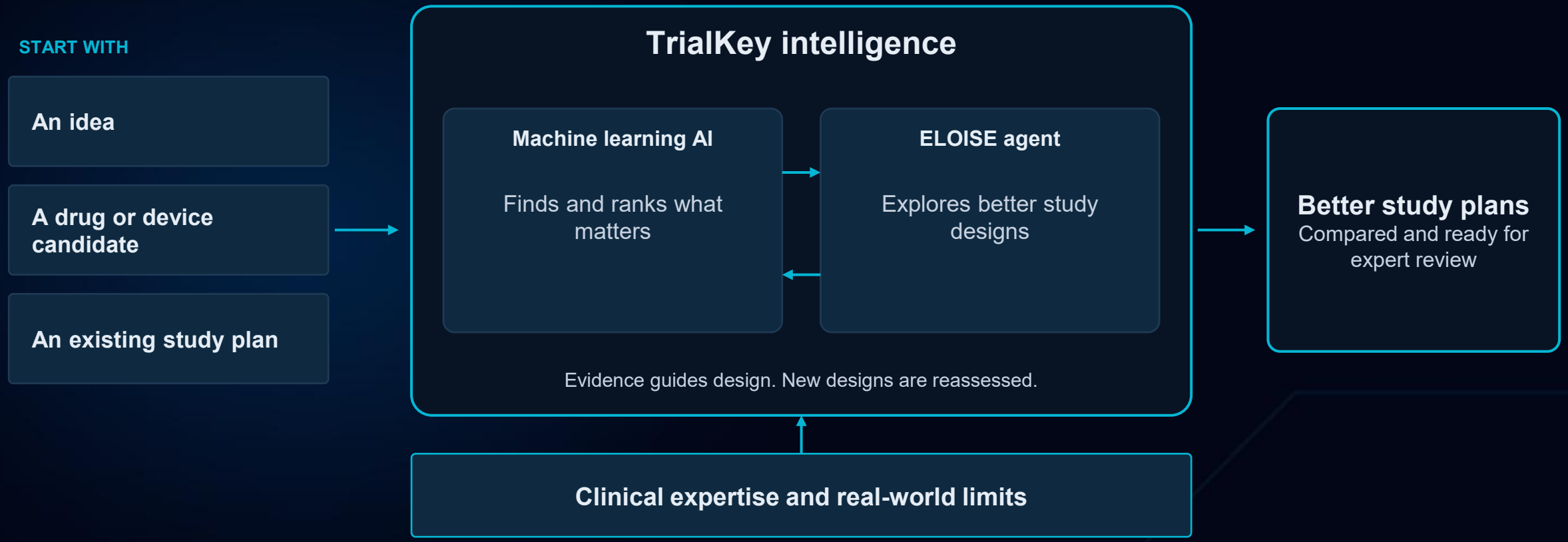
1 in 5
trials stopped before completion

TrialKey puts the risks and alternatives in front of the experts before the plan is locked, while they are cheap to fix.

Sources: TrialKey internal dataset, 27 August 2026 (88% changed plans within three years; 43% recruited less than 90% of target; timing on 6,167 of 9,480 trials with paired dates; eligible groups differ; cost impact and causes of stopping not measured). Getz et al., Tufts CSDD, 2024 (76% of protocols amended).

TrialKey helps build better study plans

Start at any stage. Use evidence to explore better designs.



What the model suggests is possible

Exploratory redesign scenarios based on 100 historical trial records

PREDICTED SUCCESS SCORE

+20.5 percentage points

Median modelled uplift

ESTIMATED TRIAL COST

31% lower

Median modelled saving
From separate cost-focused scenarios

Model predictions only. These redesigned trials have not run in real life.

No subject matter expert has assessed the proposed changes.

86 of 100 success scenarios changed primary-outcome descriptors. 85 of 100 cost scenarios reduced participant numbers without a new power calculation. Clinical feasibility remains unverified.

No demonstrated improvement in actual trial success, cost or time to market.

What we said, what we did, what is next

SAID 29 April 2026

- Complete Chipforge acquisition
- Build unique custom-silicon IP
- Add industry leaders

DID

- Placement cornerstoned by Sam Weiss, August 2026
- Built the engineering team across Australia, Singapore and India
- Independent validation of the platform, October 2026
- Advisory Board established, Prof. Anupam Chattopadhyay, September 2026
- First contract, a proof of value design underway, August 2026

NEXT - CHIPFORGE

- Chipforge Studio version 1, our first customer release version, Q3 FY2027
- Extending the FPGA tool chain into Lattice and Microchip FY2028
- Developing the custom ASIC tool chain FY2028
- Architecture and development of the secure infrastructure platform FY2028
- Fine tuning of the Chipforge LLM model release. Depending on good quality data inputs . FY2028
- Commercialisation. Paid programs converting to recurring revenue

Sources - PKY ASX announcements dated 29 April 2026, 11 August 2026, 12 August 2026, 10 September 2026, and 4 November 2026.

Funded for next stage of growth

Shares on issue
1,351.6m
1,847.0m fully diluted

Market cap
A$21.6m
at 31 October 2026 (@$0.016)

Cash in bank
A$5.8m
As at 30 September 2026

Share ownership



- **Top 20 & KMP :** 61%
- **Others:** 39%

at 31 October 2026

Board of Directors

Shannon Robinson
Chair

Damon Rasheed
Director

Paul Niardone
Director

The people building it



Andrew Farnsworth
Group CEO



Shripad Deshpande
Head of Hardware Engineering. Formerly Synopsys and Cadence



Damon Rasheed
TrialKey



Sam Weiss
Strategic adviser. Altium chair for 17 years



Prof. Anupam Chattopadhyay
Advisory Board. Chip design and AI, NTU Associate Professor

ENGINEERING TEAMS IN AUSTRALIA, SINGAPORE AND INDIA · CORE TECHNICAL CAPABILITIES

Software engineering
The platform, the record and the tool chain translators

AI and agentic model development
The agents, the loops and the fine tuned model

Hardware development and engineering
FPGA and custom silicon design, verification and test on hardware

Five things to take away: Custom silicon sits underneath everything that matters.

TAKE AWAY

01 **It works.**
The Chipforge platform takes an engineer's intent through to a verified design on real hardware, proven independently and measured against public industry benchmarks. This is what we said we would build.

02 **It is built for the customer.**
Chipforge enables the customer's design to be developed on the right hardware for the project. The design, the record and the knowledge belong to the customer, and the platform runs where the data has to live, from public cloud to fully air-gapped.

03 **The region needs it.**
The Asia Pacific region needs to move from making chips to designing them, and Australia has made sovereign capability a national priority. Chipforge, built in Singapore and Australia, is a design layer for both.

04 **The next year is about revenue.**
Chipforge Studio to customers, more tool chains, the custom silicon path, the secure platform and the fine tuned model, with paid programs converting to recurring revenue. Intentions, worked toward, reported as they land.

05 **TrialKey is proving its model.**
Trial plans change nine times in ten. TrialKey puts the alternatives in front of the experts first, and the next step is validating its redesigns with clinicians.

You cannot hire your way to design a chip. The world will be more than a million chip engineers short by 2030, and the gap is widest where the chips are made.

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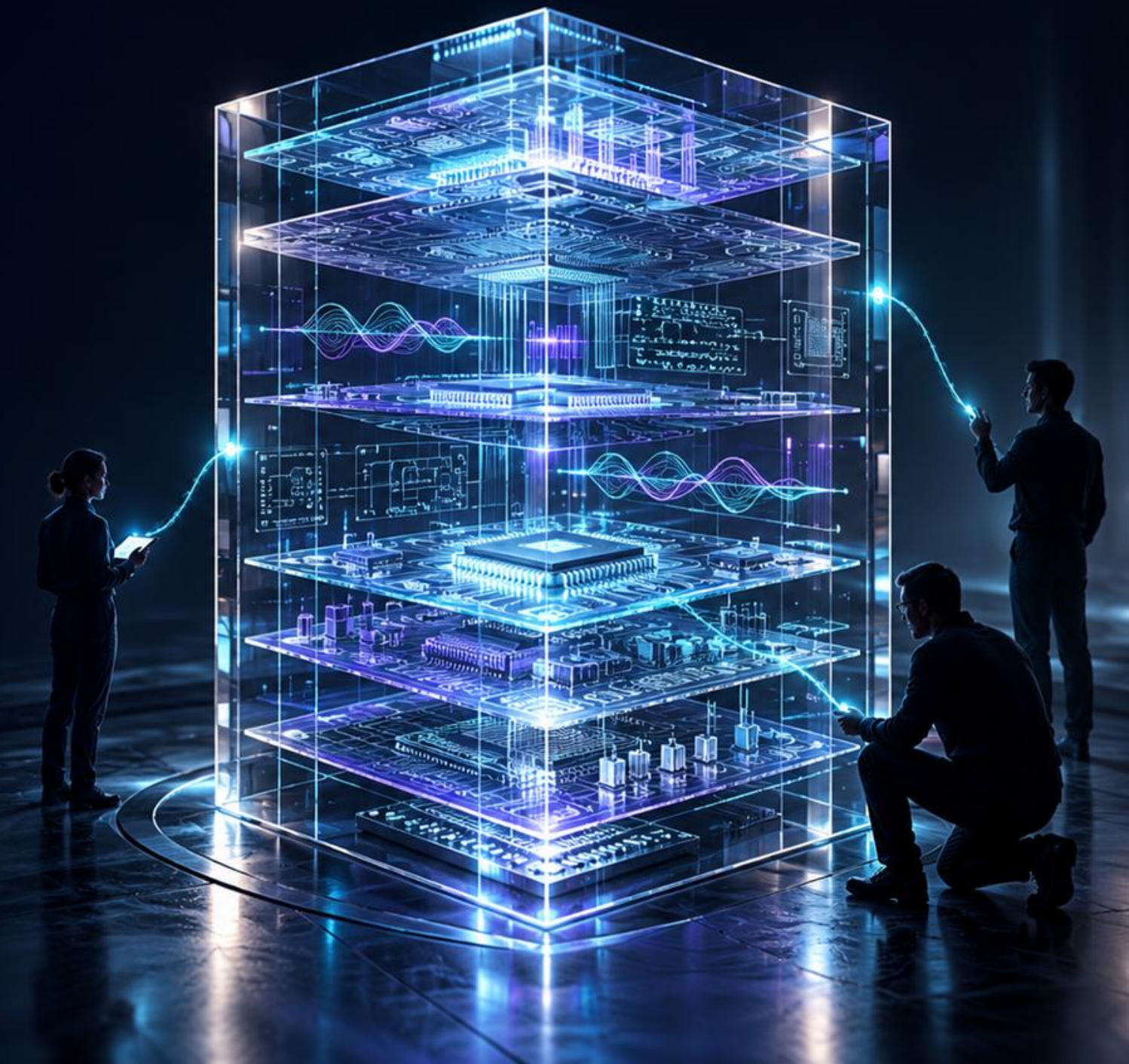
Thank you.

Investor enquiries:

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We welcome your questions and continued support.

Chipforge TrialKey



Terms used

FPGA	Field-Programmable Gate Array: a chip whose internal logic can be reprogrammed after it is manufactured. Where most Chipforge designs start.
Custom silicon	An ASIC (Application-Specific Integrated Circuit): a chip built for one fixed purpose. Cheaper and faster at high volume, but costly to design and unchangeable once made.
EDA	Electronic Design Automation: the specialist software used to design, simulate and verify semiconductor chips. The market Chipforge operates in.
RTL	Register-Transfer Level: the hardware code that describes a chip's logic, written in languages such as Verilog or VHDL. What Chipforge writes, tests and verifies.
Bitstream	The configuration file that programs a finished design onto an FPGA, setting how its logic blocks behave and connect.
Benchmark	A public, standardised set of test problems used to compare tools or AI models on identical tasks. CVDP is NVIDIA's.
Tool chain	A vendor's integrated set of design tools, such as AMD Vivado or Synopsys Fusion Compiler. Chipforge sits above them.
Air-gapped	A system kept physically isolated from outside networks for security. The appliance edition on slide 10.

Plain-English meanings for the engineering terms in this presentation.

Chipforge

WHAT AN FPGA IS

A chip whose circuits you design yourself

Field Programmable Gate Array

You buy a blank chip from AMD, Altera, Lattice or Microchip. It arrives full of millions of tiny logic cells and wiring that connect to nothing yet. An engineer writes the design, the vendor's tool chain turns it into a configuration file, and loading that file wires the chip into exactly that circuit. From then on it behaves like a chip built for the job, with every part of the circuit running at once.

What is inside the chip

Logic cells
the raw material, millions of programmable

Block memory
small fast memories spread through the chip

DSP blocks
hardwired multipliers for signals, filters and AI maths

Transceivers
serial links at tens of gigabits for Ethernet, PCIe, fibre

Hard blocks
ready-made Ethernet, PCIe and memory controllers

Processor cores
on SoC parts, Arm CPUs and AI engines beside the logic

THE CHAMELEON. LOAD A DESIGN AND IT BECOMES ANY OF THESE, OR SEVERAL AT ONCE

FPGA
Reprogrammable
Blank logic, waiting for a design. Flexibility costs some power and area

Processor
A soft CPU such as RISC-V, running ordinary software

Microcontroller
A small core plus the timers, serial ports and IO it needs

Maths engine
DSP or GPU style pipelines, thousands of multiplies every clock

Data plane
Packets, video or sensor streams wired straight through, no software in the path

ASIC
Custom silicon
Built for one job only. Power, performance and area all optimised, no spare logic, no reprogramming

Chipforge

THE FPGAS YOU CAN BUY

From under a dollar to tens of thousands, one design flow

The chip
Bought in volume for your own board, by part number, like any other component

A board or module
Development kits and system on modules with the chip mounted and ready to run

The vendor tool chain
Vivado, Quartus, Radiant, Libero. Turns the design into the file that configures the chip

LOW COST, LOW POWER

Glue logic, sensors, wearables, battery devices.

Lattice iCE40 and Certus, AMD Spartan, Altera MAX and Cyclone

~$2 to $20

MID RANGE

Vision, industrial, automotive, medical. The volume heart of the market.

AMD Artix and Kintex, Altera Agilex 5, Microchip PolarFire

~$20 to low thousands

HIGH END

Data centre, trading, telecom, radar. The largest parts made.

AMD Virtex UltraScale+, Altera Stratix and Agilex 7

Thousands to ~$65,000

ADAPTIVE SOC

Arm processors and AI engines beside the logic. Software and hardware on one chip.

AMD Zynq and Versal, Altera Agilex SoC

Tens to ~$30,000

SPACE AND RAD HARD

Radiation tolerant parts for satellites, defence and nuclear.

Microchip RTG4 and RT PolarFire, AMD XQR Versal

Can range over $50,000

Distributor list prices in US dollars, single unit, October 2026. Every product on the next two slides uses one of these classes, and the same design moves between them and on to custom silicon.

Chipforge

WHAT AN ASIC IS

The same design, made permanent and made for one job

Application Specific Integrated Circuit

A chip whose circuit is fixed when it is manufactured. It starts as the same design that ran on the FPGA, then that design is laid out as transistors and wiring, checked, and manufactured by a foundry. It carries only the logic the job needs and nothing that is not used. Every smartphone processor, AI accelerator and hearing aid chip is an ASIC.

Why people choose one

- **Power** a fraction of the FPGA's
- **Performance** faster clocks, no programmable routing
- **Unit cost and size** a tiny die, cents to dollars at volume
- **Control** your own IP and security, nothing to read out

THE PRICE OF ADMISSION

Design, verification, sign off and the mask set are paid once, before the first chip exists. Hundreds of thousands of dollars at mature nodes, tens of millions at the leading edge.

NO SECOND CHANCES

A year or more from design to working parts. After tape out nothing can be changed, and a bug means paying for the masks again. This is why the design is proven on an FPGA first.

WHEN IT MAKES SENSE

Volume high enough to spread the upfront cost, a product that is power or size constrained, or a need to own the silicon outright. The FPGA stays where volumes are low or the design keeps changing.

Prove it on an FPGA, then freeze it. Chipforge works at the design level, so one design serves the FPGA today and the custom chip when the volume arrives.

OUR CUSTOMERS FPGA

Chipforge

Our customers use FPGAs to build the products around you



Consumer electronics

Televisions, cameras, audio, VR headsets, drones



Computing

Capture cards, docks, external storage, NAS, gaming consoles



Networking

Wi-Fi 7 routers, modems, switches, satellite terminals, small cells



Automotive

Driver assistance, lidar, instrument clusters, EV power, chargers



Home and energy

Appliances, robot vacuums, cameras, thermostats, solar inverters



Health and personal

Glucose monitors, hearing aids, handheld ultrasound, fitness, CPAP



Mobility and outdoor

E-bikes, marine chartplotters, GPS messengers, launch monitors



Retail and public spaces

Payment terminals, self checkout, signage, kiosks, access gates

Every one of these runs on an FPGA or custom silicon. The teams who design them are the teams Chipforge is built for.

Chipforge

FPGA MISSION CRITICAL AND INFRASTRUCTURE

Where latency, security and uptime decide the product

Data centre and cloud

SmartNICs and DPUs, data planes, inference accelerators, storage

Financial trading

Ultra low latency trading, market data feeds, risk and order gateways

Telecom infrastructure

5G baseband and fronthaul, optical transport, core routers

Defence and aerospace

Radar, electronic warfare, secure communications, avionics

Space and satellite

Payload processing, ground stations, radiation tolerant control

Security and sovereign

Encryption, cross domain gateways, hardware security modules

Industrial and robotics

Motion control, machine vision, PLCs, test and measurement

Medical and scientific

MRI and CT imaging, gene sequencers, physics detectors, oscilloscopes

These platforms live or die on microseconds, uptime and data that cannot leave the building. They are the deepest users of FPGAs and custom silicon, and the teams building them are the customers Chipforge's secure editions are built for.