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Who is Adisyn

Adisyn Ltd is publicly listed on the Australian Securities Exchange (ASX) under the ticker AI1

(ASX:AI1) 



01

2D Generation

A fully owned subsidiary. Development of novel technologies to produce graphene in a low-temperature process, targeting semiconductors.



02

2D Radar Absorbers

A subsidiary of 2D Generation. Radar signature reduction for UAV and defence systems, using 2D materials.



03

IT and cyber security

The original activity of building and deploying IT solutions, and end-to-end cyber security solutions.

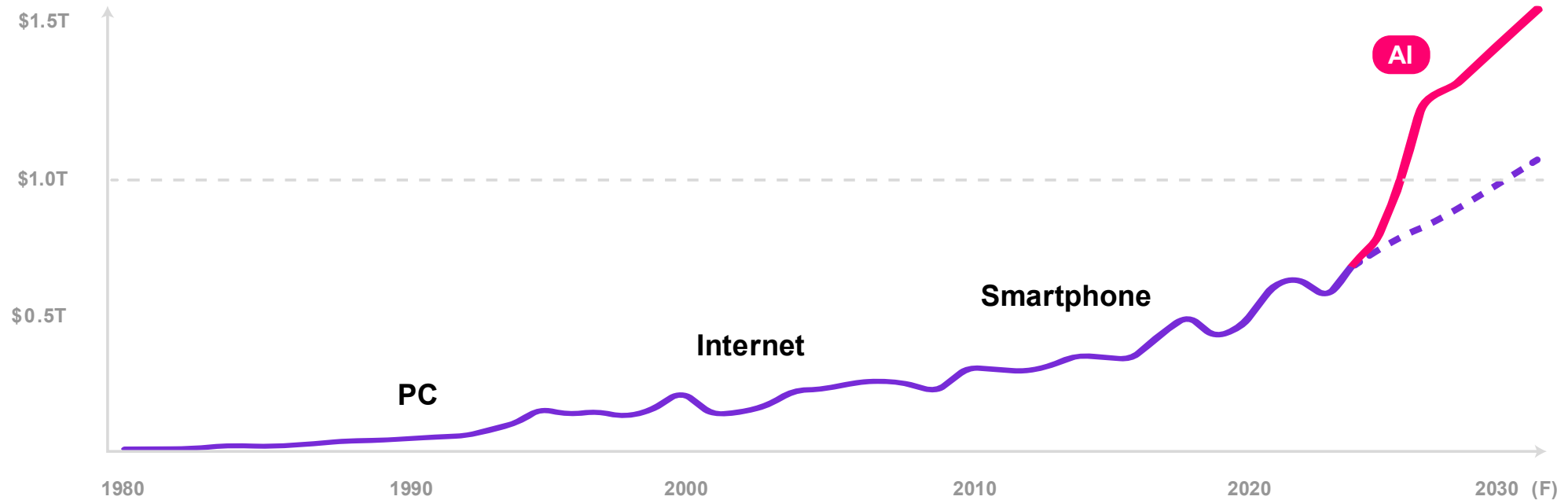
CORPORATE SNAPSHOT

Share price, 21/09/26	A\$0.14
Market cap, 21/09/26	c. A\$165M
Cash, 30/06/26	c.A\$15.5M

BOARD OF DIRECTORS

Kevin Crofton	Executive Chairman
Arye Kohavi	Non-Executive Director
Dominic O’Hanlon	Non-Executive Director
Blake Burton	Executive Director

Semiconductor \$1T Milestone Accelerated



\$1.0T

Milestone crossed

The industry passes one trillion dollars this decade.

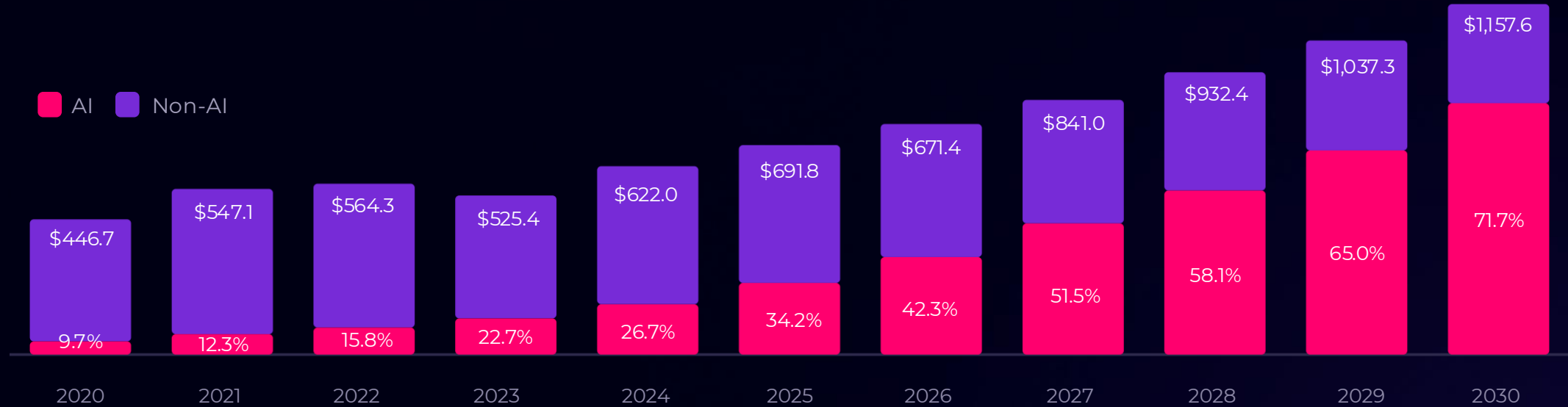


\$1.5T

By 2030 (F)

AI is what pulls the curve above the earlier forecast.

The AI market drives the semiconductor ecosystem



Source: IBS, February 2025. In billion \$.



\$1,157.6 Billion by 2030

Up from \$446.7B in 2020.

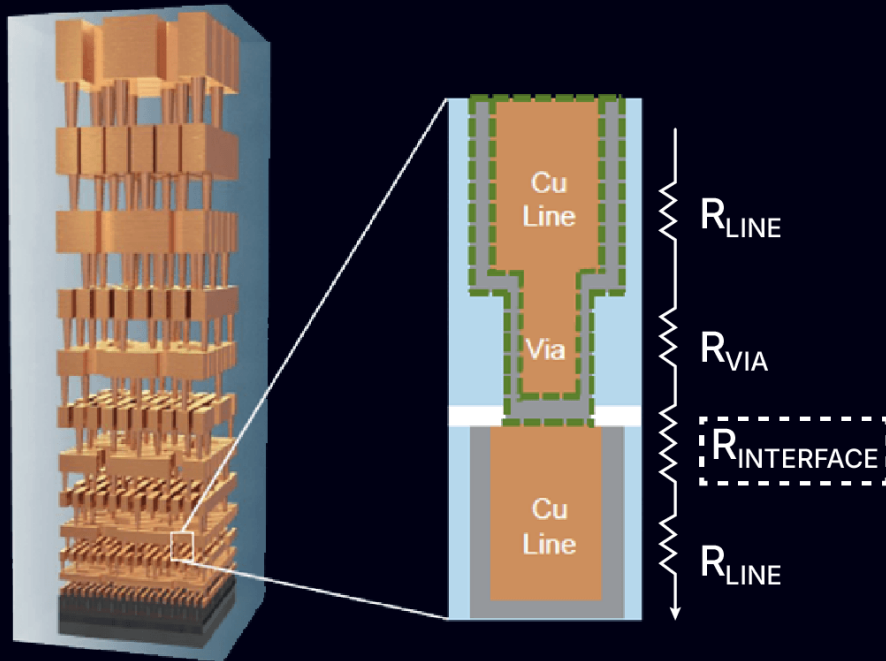


71.7% AI share by 2030

It was 9.7% in 2020.

High Performance Computing's Primary Barrier

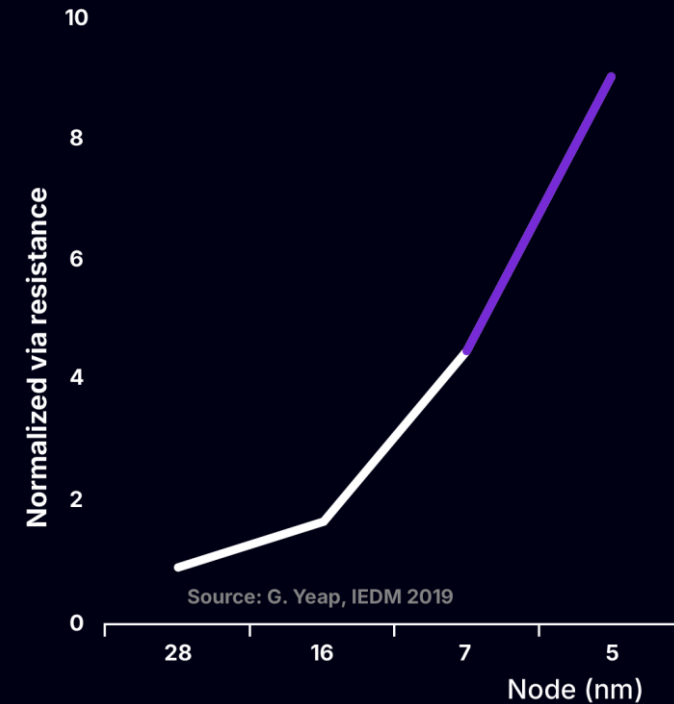
Interfaces contributes >50% of resistance



>5 interfaces at narrow via-line connections

Atomic-level nucleation and termination of interfaces

Resistance (R) escalates at small dimensions



Higher resistance = higher dynamic power loss

>1/3rd of chip power is consumed in

WHAT THE INDUSTRY NEEDS

Industry Must-Have Solutions

To support the coming demands.
Requirements for high performance,
low power AI semiconductors.



Five requirements, one constraint
They all run into the same interconnect limit.



High Performance

Increasing speed of device

01



Low Power

Reducing power consumption

02



High Density

Smaller chips or stacked chips, to process more data

03



High Bandwidth

Transmission of large amounts of data at once

04



Low Latency

Connection pathway of data transmission without delay

05

2D GENERATION PROCESS

<450°C

A unique and patented process,
compatible with fab constraints

Atomic Layer Deposition (ALD) based, low-temperature, using readily available precursors, and applicable with existing industrial processes and equipment.



Unique and patented process

Four patent families sit behind it.



Compatible with fab constraints

ALD based. Low-temperature, well below 450°C. Uses readily available precursors.



Existing industrial equipment

Can be applied using industrial processes and equipment that fabs already run.

Expanding IP Coverage Across the Graphene Interconnect Stack

Third Patent Extends Adisyn's Graphene IP into Non-metallic Surfaces

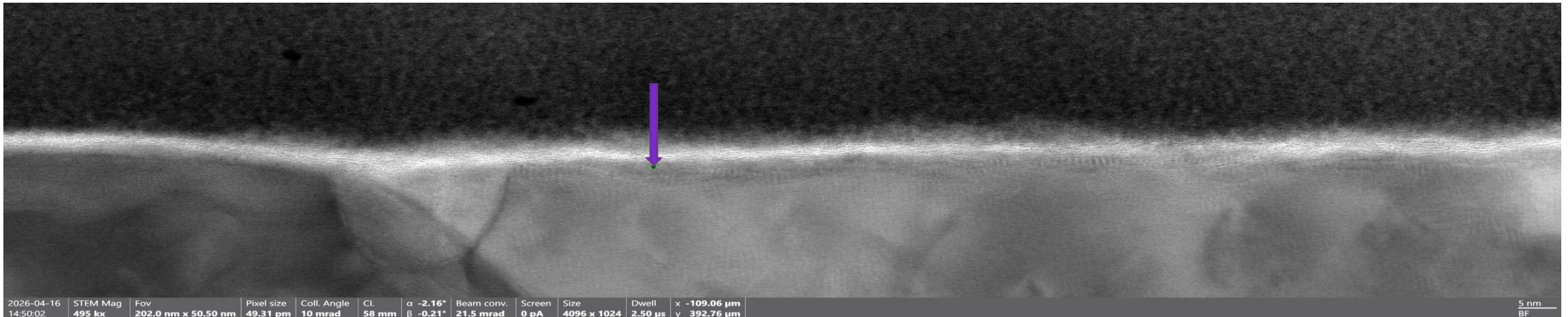
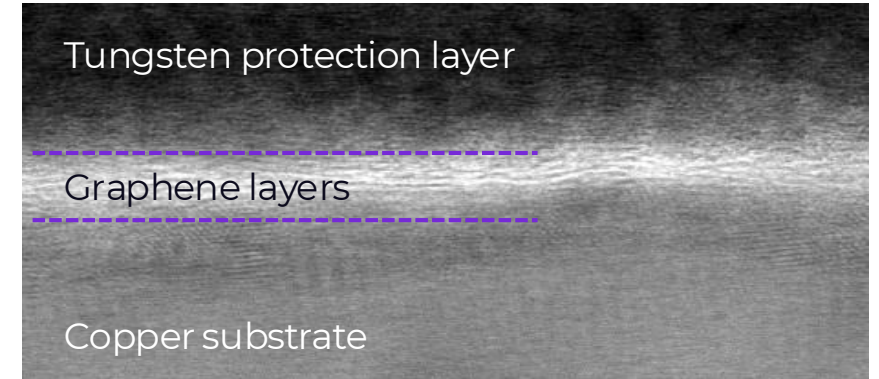
- Patents 1 & 2: Cover graphene deposition onto **metallic surfaces** and resulting metal-based interconnect products.
- Patent 3: Extends protection to direct graphene deposition on **non-metallic surfaces**, including interconnect structures where graphene acts as the diffusion barrier between the conductor and surrounding dielectric (including sidewalls).
- Together, the patent portfolio potentially provides **IP coverage “across both sides of the barrier interface.”**
- This creates **multiple potential points of IP relevance** as the semiconductor industry seeks to integrate graphene into conventional interconnect manufacturing.
- Industry validation: imec has investigated graphene as an ultrathin diffusion barrier, highlighting characteristics including atomic-scale thickness, high current-carrying capacity, thermal conductivity and electromigration performance.



All is building an IP position around both the process of depositing graphene and its integration into next-generation semiconductor interconnect structures.

Successful Deposition of Continuous Layer Of Graphene at Low Temperature

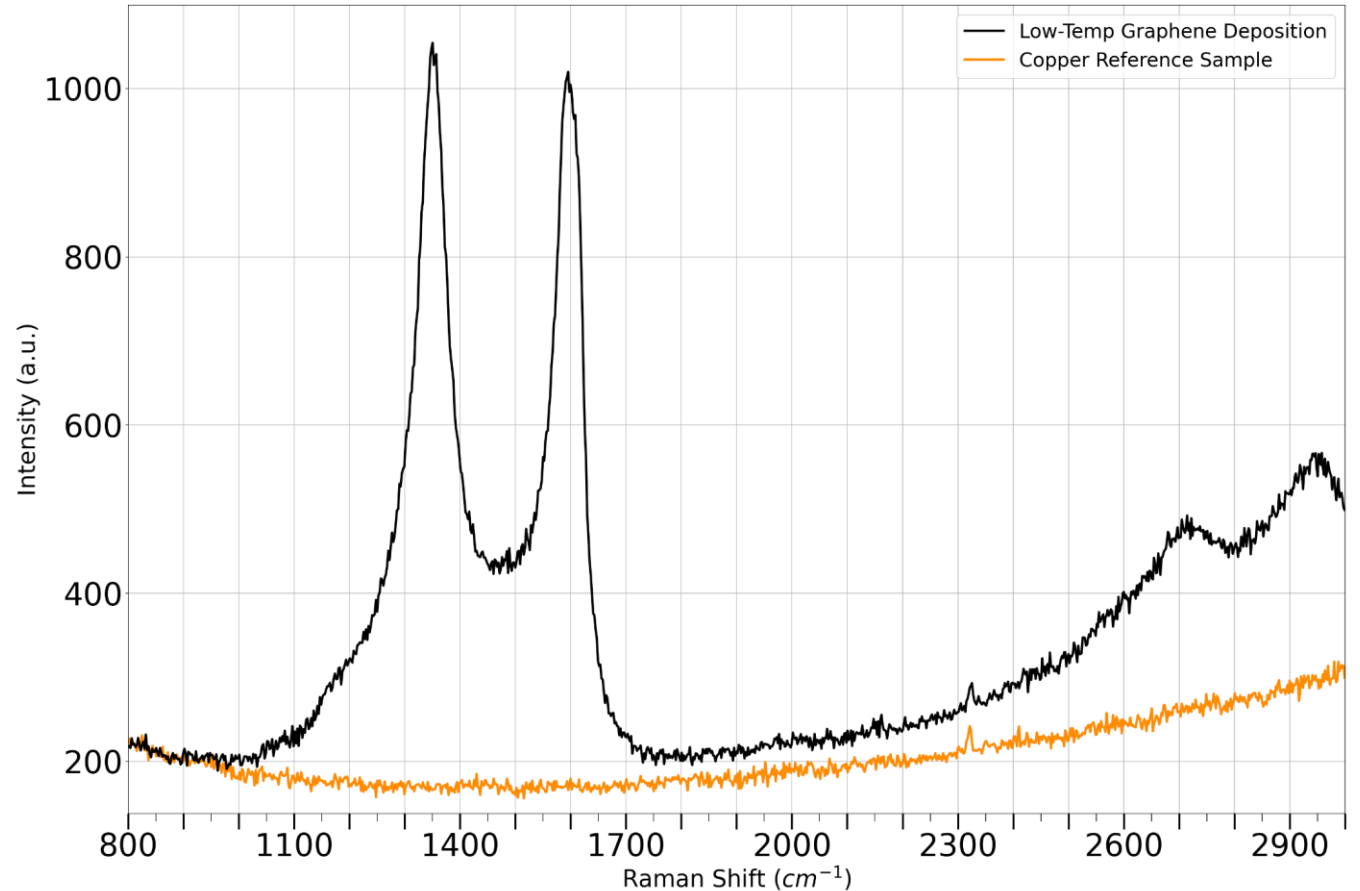
$\sim 1 \text{ nm}$ layer of graphene,
 $d = 3.4 \pm 0.3 \text{ \AA}$



THE PROOF

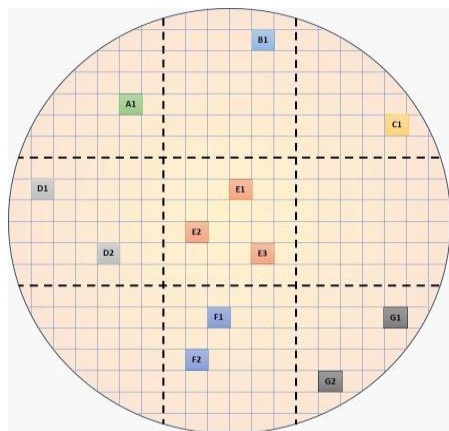
Raman Analysis – Low-temp PEALD Graphene Deposition on Copper Substrate

The low-temp deposition shows both. The copper reference sample shows neither.

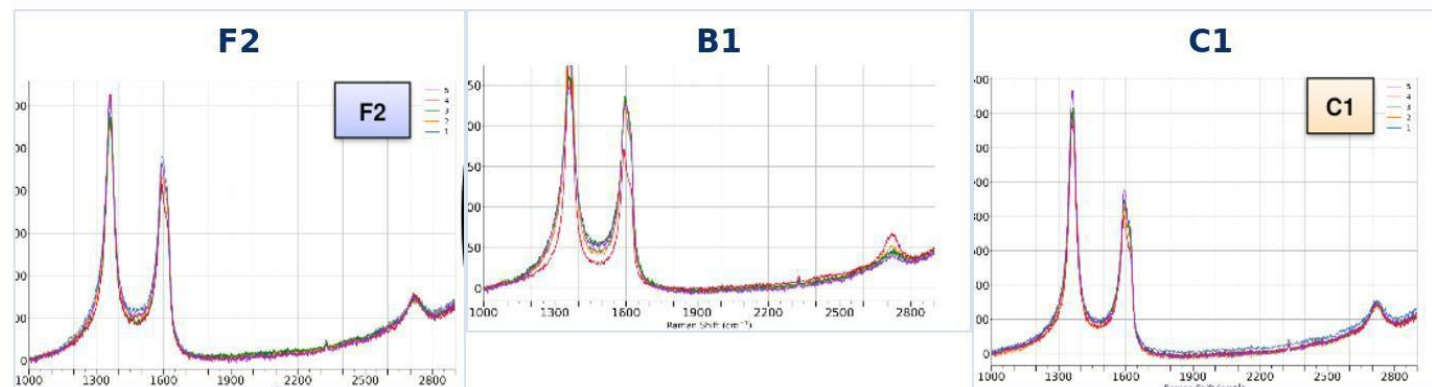


August 2026: Scale-up milestone on a 200mm wafer

Independent tests confirmed graphene across 12 sampled locations.



Representative Raman spectra (five measurements per location)



12 of 12



Sampled locations confirmed

5



Measurements per location

200mm



Wafer

WHAT THE 200MM RESULT MEANS

7.7M (~2M SAM)

wafer starts a month, and a
path to potential first revenue

Around 20 to 30% of that would represent our Serviceable Addressable Market (SAM) for graphene, at potentially lower risk for adoption than leading-edge logic.

Source: Semi 200MM Fab Outlook Report

Scale



Immediate indication of potential to scale to 300mm, critical for AI and HPC devices.

Specialty device makers



Opens the avenue to engage with specialty device makers, with Significant TAM of 7.7M wafer starts per month

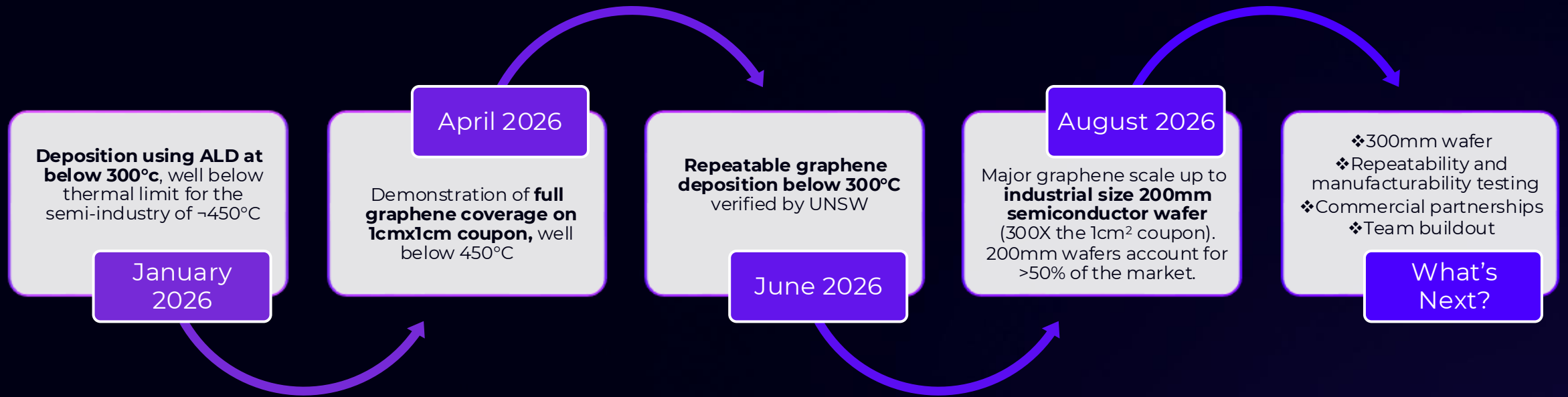
An economic play



Power semiconductors, RF & MEMS, advanced sensors, even potentially analog.

- C. 20–30% would represent our SAM for graphene

Hitting milestones at increasing velocity



Highly Scalable Revenue Model

From Patent Portfolio → Non-Recurring Engineering Revenue → Low-Rate Production → Industry Adoption → Recurring Royalties

Illustrative royalty economics — US\$10 per wafer

Annual wafers using technology	Illustrative annual royalty revenue*
1 million	US\$10m
10 million	US\$100m
50 million	US\$500m

Approximately 95–105 million 300mm wafers are expected to be produced in 2026, potentially increasing to 130–140 million annually by 2030, which excludes the substantial 200mm wafer market.

**Illustrative only. Not a forecast or indication of expected pricing, adoption or revenue.* Source: Semi 300MM Fab Outlook Report



Additional scalable route to market

Alongside licensing directly to manufacturers such as TSMC, Samsung or Intel, Adisyn's graphene deposition process could potentially be integrated into semiconductor deposition equipment → reaching multiple foundries and chip customers.



Appendix

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Intellectual Property

Four patent families covering the interconnect including both sides of the barrier interface.



01

Graphene coated non-metallic surfaces, devices and method thereof

Directed to the technologies used for conductive diffusion barrier, and other applications.



02

Graphene coated metallic surfaces, devices and method of manufacture thereof

Directed to the technologies used for conductive capping layer, and other applications.



03

Method of manufacture of graphene coated surfaces by atomic or molecular layer deposition

Directed to graphene manufacture by ALD.



04

Graphene metal composite

Directed to graphene layers interlayered with metal layers, including coatings of patterned surfaces.

Proven business models used in the semi industry



Process platform plus running royalty

The classic approach, but with the lowest potential revenue.



Large paid technology transfer / joint-development programme

Long programme, large revenue and very long timelines. For example IBM through the 1990s, 2000s and into the 2010s.



Staged licence

Evaluation, then R&D, then HVM, then per-wafer or per-device royalty. The model used by Soitec, Atomera and in the ST / Infineon / IBM copper example.

Multi-band Radar Systems Detect UAVs Earlier Than Ever

How modern radar systems detect uavs

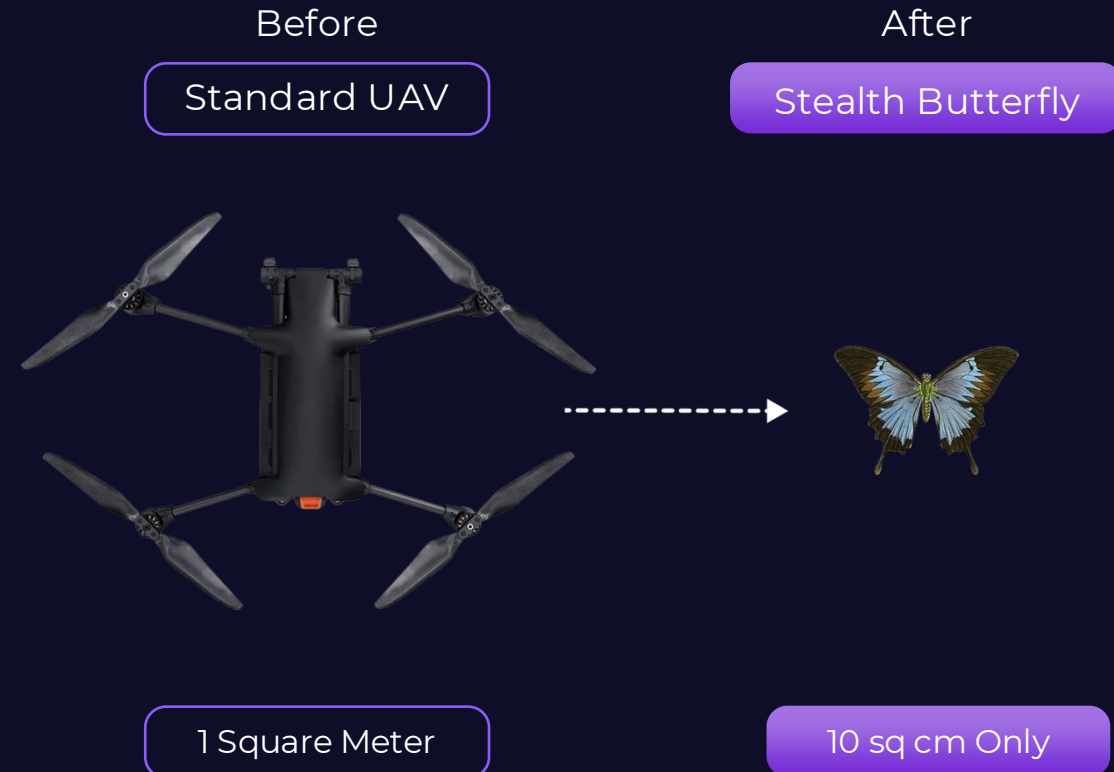
- Transmits a pulse of radio frequencies
- The signals hit an object, for example a UAV
- Part of the signal is reflected back to the radar receiver
- The radar measures the strength of the returned signal

Signal strength is expressed in decibels



Decibels are a logarithmic scale and a 30dB reduction can equate to a 1,000x decrease in radar signature.

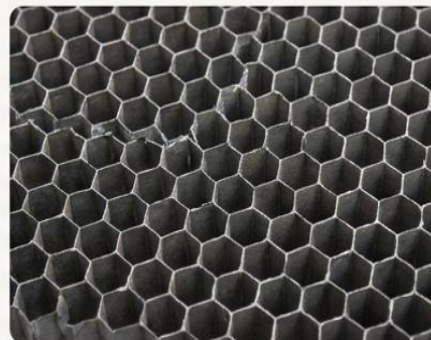
The Physical Meaning of 30dB: Reducing Radar Signature by 1,000 Times



The Adisyn Solution

Graphene-enhanced structural components which are light, strong and possess significant radar-absorbing properties.

Proven Feasibility: 20dB Goal Successfully Achieved in Lab



Current Achievement:

Proven 20dB Reduction

20dB with graphene composites compared to base materials

Successfully Completed

Proven reduction in radar signal return

Optimization Goal:

30dB

Optimization target for 12.2026



Proof-of-concept result: 20dB reduction, a 100-fold decrease in radar return, successfully achieved in the lab by integrating advanced 2D graphene materials directly into the printed plastic matrix.



Ongoing optimisation targeting ~30dB radar signature reduction, which can equate to a 1,000-fold decrease in radar return. This substantially surpasses current conventional products and would permit access to higher-margin markets.



Thank You

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